MMAGRxxGUECx - xMBxx
MMAGFxxGWECx - xMBxx

Final

Samsung SD & MicroSD Card product family

SDA 3.0 specification compliant-Up to High Speed mode

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	1. Initial issue	Jan. 20, 2010	Draft	S.M.Lee
0.5	1. Assorted by NAND Flash version. 2. Engineering Sample acquired	Jan. 26, 2010	Preliminary	S.M.Lee
1.0	1.CCC and WP_GRP_ENABLE Register are Changed	Mar. 2, 2010	Final	S.M.Lee
1.1	1.SD Card 2Gb is added	Mar. 18, 2010	Final	S.M.Lee

Table Of Contents

1.0 INFORMATION

M	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1. Module: M

2. Module Configuration
   C : Flash Card (SLC)
   E : Flash Card (OneNAND)
   M : Flash Card (MLC)

3~4. Flash Density

64 : 64M	28 : 128M
56 : 256M	2 : 512M
5D : 512M DDP	1G : 1G
1D : 1G DDP	2G : 2G
2D : 2G DDP	4G : 4G
8G : 8G	AG : 16G
B3 : 32Gb 3bit	BG: 32Gb 2bit

5. Feature
   R : microSD
   F : SD

6~8. Card Density

008 : 8M Byte	016 : 16M Byte
032 : 32M Byte	048 : 48M Byte
064 : 64M Byte	096 : 96M Byte
128 : 128M Byte	192 : 192M Byte
256 : 256M Byte	384 : 384M Byte
512 : 512M Byte	01G : 1G Byte
02G : 2G Byte	04G : 4G Byte
08G : 8G Byte	16G : 16G Byte
32G : 32G Byte	

9. Card Type
   U : microSD
   W : SD

10. Component Generation

M : 1st Generation	A : 2nd Generation
B : 3rd Generation	C : 4th Generation
D : 5th Generation	E : 6th Generation

11. Flash Package

C : CHIP	Y : TSOP1
V : WSOP	B : TBGA

12. PCB Revision and Production site.

A : None (SEC)	B : 1st Rev. (SEC)
C : 2nd Rev. (SEC)	D : 3rd Rev. (SEC)
P : None (STS)	Q : 1st Rev. (STS)
R : 2nd Rev. (STS)	U : None(ATP)
V : 1st Rev.(ATP)	W : 2nd Rev.(ATP)
Y : None(SPIL)	

13. " - "

14. Packing Type
   0 : With Label
   1 : Without Label / Contents
   2 : No Label
   3 : With Components / No Label
   4 : Bulk Type I (only Back Label)
   5 : Bulk Type II (only Back Label)

15 ~ 16. Controller
   MB: SS6627AAWWE

17 ~ 18. Customer Grade
   " Customer List Reference "

2.0 PRODUCT LINE-UP

Model Number	Capacities	Remarks
MMAGR02GUECx - xMBxx	2GB	SD / micro SD Card (x : Refer to the Ordering Information)
MMAGF02GWECx - xMBxx	2GB	

3.0 INTRODUCTION

3.1 General Description

The SD/microSD is a memory card that is specifically designed to meet the security, capacity, performance and enviroment requirements inherent in newly emerging audio and video consumer electronic devices. The SD/microSD will include a copyright protection mechanism that complies with the security of the SDMI standard and will be faster and capable for higher Memory capacity. The SD/microSD security system uses mutual authentication and a "new ciper algorithm" to protect from illegal usage of the card content. A none secured access to the user's own content is also available. The SD/microSD communication is based on an advanced 9 and 8-pin interface (SD:9pin, microSD:8pin)) designed to operate in at maximum operating frequency of 208MHz and 2.7V ~ 3.6V voltage range with 2 Type signaling(1.8V & 3.3V)*. More detail informations on the interface, and mechanical description is defined as a part of this specification.

* High Speed mode Limited on this Specification.

3.2 System Features

- Compliant with SD Memory Card Specifications PHYSICAL LAYER SPECIFICATION Version 3.00
  - Based on SD Memory Card Specification 3.0 compatible Test Device.
  - Bus speed only support up to High Speed Mode (3.3V signaling, frequency up to 50MHz)

- Targeted for portable and stationary applications
- Memory capacity:
  1) Standard Capacity SD Memory Card(SDSC) : Up to and including 2 GB
  2) High Capacity SD Memory Card(SDHC) : More than 2GB and up to and including 32GB
  3) Extended Capacity SD Memory Card(SDXC) : More than 32GB and up to and including 2TB

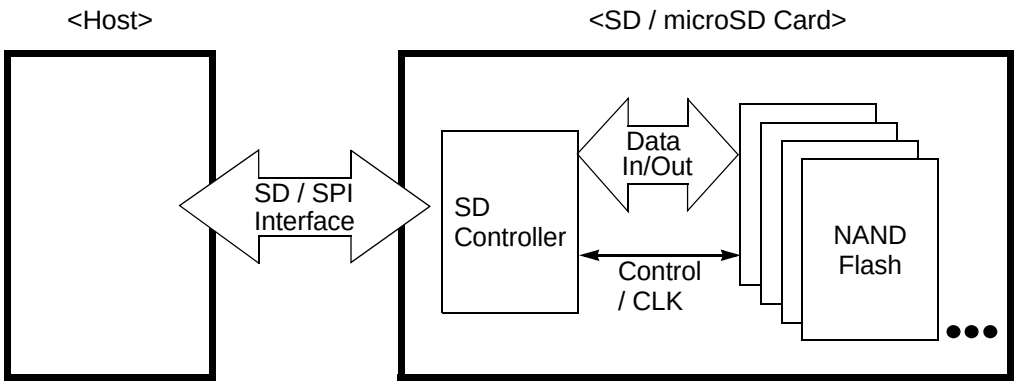
- Voltage range:
  High Voltage SD Memory Card – Operating voltage range: 2.7-3.6 V

- Designed for read-only and read/write cards.

- Bus Speed Mode
  1) Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed (using 4 parallel data lines)
  2) High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25 MB/sec interface speed (using 4 parallel data lines)

- Switch function command supports High-Speed, and future functions
- Correction of memory field errors
- Card removal during read operation will never harm the content
- Content Protection Mechanism - Complies with highest security of SDMI standard.
- Password Protection of cards (CMD42 - LOCK_UNLOCK)
- Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Card Detection (Insertion/Removal)
- Application specific commands
- Comfortable erase mechanism
- Weight : SD Card Max. 2.5g / microSD Card Max. 1g

3.3 System Block Diagram



4.0 PRODUCT SPECIFICATION

4.1 Current Consumption

This information table below provides current consumption of Samsung SD/microSD Card. Current consumption is measured by averaging over 1 second.

[Table 4-1] : Current Consumption Table

Mode	Max. Interface Frequency	Operations	Max.
Default Mode	25Mhz	Read	100mA
		Write	
High Speed Mode	50Mhz	Read	200mA
		Write	

* Current consumption on each device can be varied by NAND Flash, number of chips, test conditions and Etc. For specific information, refer to Samsung SD/microSD Card Qualification report.

4.2 System Performance

4.2.1 Product Performance & Speed Class Information

Product Performance and Speed Class Informations are based on TestMetrix compliance Tool. Note that the performance measured by TestMetrix does not represent real performance in various circumstances.

[Table 4-2] : Performance Information

Product Number	Write Performance (MB/s)	Read Performance (MB/s)	Speed Class*
MMAGR02GUECx - xMBxx	Typ. 4.5	Typ. 14	4
MMAGF02GUWCx - xMBxx			

* Five Speed Classes are defined and indicate minimum performance of the cards in Speed Class Test Mode. Speed Class compliant SDA Physical Layer Specification, Version 3.00

.Class 0 - These Class cards do not specify performance. It includes all the legacy cards prior to this specification, regardless of its performance
.Class 2 - is more than or equal to 2MB/s performance
.Class 4 - is more than or equal to 4MB/s performance
.Class 6 - is more than or equal to 6MB/s performance
.Class 10 - is more than or equal to 10MB/s performance

4.2.2 Read, Write Timeout Error Conditions

SEC SD/microSD Card shall complete the command within the time period defined as follows or give up and return and error message. If the host does not get any response with the given timeout it should assume that the card is not going to respond and try recover. For more information, refer to Section 4.6 of the SDA Physical Layer Specification, Version 3.00

[Table 4-3] : Timeout Error Conditions

Timing	Max. Value
Block Read Access Time	100ms
Block Write Access Time	250ms(SDSC/SDHC), 500ms(SDXC)
Initialization Time out(ACMD 41)*	1s

* The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

4.3 SD Mode Card Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

4.3.1 OCR Register

• The 32-bit operation conditions register stores the V_{DD} voltage profile of the card. Additionally, this register includes status information bits. See Section 5.1 of the SDA Physical Layer Specification, Version 3.00 for more information.
[Table 4-4] : OCR Register Definition

OCR bit	VDD Voltage Window	OCR Value
0-3	reserved	0
4	reserved	0
5	reserved	0
6	reserved	0
7	reserved for Low Voltage Range	0
8	reserved	0
9	reserved	0
10	reserved	0
11	reserved	0
12	reserved	0
13	reserved	0
14	reserved	0
15	2.7 - 2.8	1
16	2.8 - 2.9	1
17	2.9 - 3.0	1
18	3.0 - 3.1	1
19	3.1 - 3.2	1
20	3.2 - 3.3	1
21	3.3 - 3.4	1
22	3.4 - 3.5	1
23	3.5 - 3.6	1
24[3]	Switching to 1.8V Accepted (S18A)	0
24 - 29	reserved	0
30	Card Capacity Staus(CCS)[1]	-
31	Card power up status bit(busy)[2]	-

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.
3) Only UHS-I card supports this bit.

4.3.2 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have an unique identification number. It is programmed during manufacturing and cannot be changed by card hosts. The structure of the CID register is defined in the following paragraphs:

[Table 4-5] : CID Register Fields

Name	Field	Type	Width	CID Value	
				microSD	SD
				2GB	2GB
Manufacturer ID	MID	Binary	8	CID Register Value can be provided by Customer Request	
OEM/Application ID	OID	ASCII	16		
Product name	PNM	ASCII	40		
Product revision	PRV	BCD	8		
Product serial number	PSN	Binary	32		
Reserved	-	-	4		
Manufacturing date	MDT	BCD	12		
CRC7 checksum	CRC	Binary	7		
not used, always '1'	-	-	1		

4.3.3 CSD Register (CSD Version 1.0)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W=multiple writable.

[Table 4-6] : The CSD Register Fields (CSD Version 1.0)

Name	Field	Width	Cell Type	CSD-slice	CSD Value	
					microSD	SD
					2GB	2GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	Ver.1.0	
Reserved	-	6	R	[125:120]	-	
Data read access-time 1	TAAC	8	R	[119:112]	80mS	
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	25500 cycles	
Max. Data transfer rate	TRAN_SPEED	8	R	[103:96]	25 Mbit/sec or 50 Mbit/sec	
Card command classes	CCC	12	R	[95:84]	class 0 2 4 5 7 8 10	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	1024 Bytes	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	1	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	-	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	-	
DSR implemented	DSR_IMP	1	R	[76:76]	-	
Reserved	-	2	R	[75:74]	-	
Device size	C_SIZE	12	R	[73:62]	3819	
Max. read current @ V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]	60.0 mA	
Max. read current @ V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]	80.0 mA	
Max. write current @ V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]	60.0 mA	
Max. write current @ V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]	80.0 mA	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	MULT=512	
Erase single block enable	ERASE_BLK_EN	1	R	[46:46]	1	
Erase sector size	SECTOR_SIZE	7	R	[45:39]	64 blocks	
Write protect group size	WP_GRP_SIZE	7	R	[38:32]	128 sectors	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	-	
Reserved (Do Not Use)		2	R	[30:29]	-	
Write speed factor	R2W_FACTOR	3	R	[28:26]	8	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	1024 Bytes	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0	
Reserved	-	5	R	[20:16]	-	
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]	-	
Copy flag (OTP)	COPY	1	R/W(1)	[14:14]	-	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	-	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	-	
File format	FILE_FORMAT	2	R/W(1)	[11:10]	-	
Reserved		2	R/W	[9:8]	-	
CRC	CRC	7	R/W	[7:1]	-	
Not used, always '1'	-	1	-	[0:0]	-	

4.3.4 CSD Register (CSD Version 2.0)

The following Table shows Definition of the CSD Version 2.0 for the High Capacity SD Memory Card and Extended Capacity SD Memory Card. The following sections describe the CSD fields and the relevant data types for the High Capacity SD Memory Card.

CSD Version 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

[Table 4-7] : The CSD Register Fields (CSD Version 2.0)

Name	Field	Width	Cell Type	CSD-slice	CSD Value	
					microSD 2GB	SD 2GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	N/A	
Reserved	-	6	R	[125:120]	-	
Data read access-time	(TAAC)	8	R	[119:112]	N/A	
Data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	R	[111:104]	N/A	
Max. Data transfer rate	(TRAN_SPEED)	8	R	[103:96]	N/A	
Card command classes	CCC	12	R	[95:84]	N/A	
Max. read data block length	(READ_BL_LEN)	4	R	[83:80]	N/A	
Partial blocks for read allowed	(READ_BL_PARTIAL)	1	R	[79:79]	N/A	
Write block misalignment	(WRITE_BLK_MISALIGN)	1	R	[78:78]	N/A	
Read block misalignment	(READ_BLK_MISALIGN)	1	R	[77:77]	N/A	
DSR implemented	DSR_IMP	1	R	[76:76]	N/A	
Reserved	-	6	R	[75:70]	-	
Device size	C_SIZE	22	R	[69:48]	N/A	
Reserved	-	1	R	[47:47]	-	
Erase single block enable	(ERASE_BLK_EN)	1	R	[46:46]	N/A	
Erase sector size	(SECTOR_SIZE)	7	R	[45:39]	N/A	
Write protect group size	(WP_GRP_SIZE)	7	R	[38:32]	N/A	
Write protect group enable	(WP_GRP_ENABLE)	1	R	[31:31]	N/A	
Reserved	-	2	R	[30:29]	-	
Write speed factor	(R2W_FACTOR)	3	R	[28:26]	N/A	
Max. write data block length	(WRITE_BL_LEN)	4	R	[25:22]	N/A	
Partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	R	[21:21]	N/A	
Reserved	-	5	R	[20:16]	-	
File format group	(FILE_FORMAT_GRP)	1	R	[15:15]	N/A	
Copy flag (OTP)	COPY	1	R/W(1)	[14:14]	N/A	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	N/A	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	N/A	
File format	(FILE_FORMAT)	2	R	[11:10]	N/A	
Reserved		2	R	[9:8]	-	
CRC	CRC	7	R/W	[7:1]	N/A	
Not used, always '1'	-	1	-	[0:0]	N/A	

4.3.5 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the *Stand-by State* with CMD7.

4.3.6 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on SD Card's special features that were configured into the given card. The size of SCR register is 64bit. The register shall be set in the factory by the SD Card manufacturer. The following table describes the SCR register content.

[Table 4-8] : The SCR Fields

Name	Field	Width	Cell Type	SCR-slice	SCR Value	
					microSD	SD
					2GB	2GB
SCR structure	SCR_STRUCTURE	4	R	[63:60]	Version 1.01-3.00	
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]	Version 2.00 or 3.00	
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]	-	
SD Security Support	SD_SECURITY	3	R	[54:52]	Ver. 1.01	
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]	1bit(DAT0) & 4bit(DAT0-3)	
Spec. Version 3.00 or Higher	SD_SPEC3	1	R	[47]	Version 3.0	
Reserved		13	R	[46:34]	-	
Command Support bits	CMD_SUPPORT	14	R	[33:32]	0	
Reserved for manufacturer usage	-	32	R	[31:0]	-	

4.3.7 SD Status Register

The SD Status contains status bits that are related to the SD Memory Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran_state' (card is selected). SD Status structure is described in below. Unused reserved bits shall be set to 0.

[Table 4-9] : SD Status Register

Bits	Field	Cell Type	Data		Value	
			microSD 2GB	SD 2GB	microSD 2GB	SD 2GB
511:510	DATA_BUS_WIDTH	S R	0x00 or 0x10		1 bit width or 4bit width	
509	SECURED_MODE	S R	0x00		-	
508:502	Reserved for Security Runctions (Refer to Part 3 Security Specification)					
501:496	Reserved		0x0		-	
495:480	SD_CARD_TYPE	S R	0x0000		Regular SD RD/WR Card	
479: 448	SIZE_OF_PROTECTED_AREA	S R	0x28		-	
447:440	SPEED_CLASS	S R	0x2		Class 4	
439:432	PERFORMANCE_MOVE	S R	0x2		2 [MB/s]	
431:428	AU_SIZE	S R	0x9		4MB	
427:424	Rserved					
423:408	ERASE_SIZE	S R	0x10		16 AU	
407:402	ERASE_TIMEOUT	S R	0x1		1 sec	
401:400	ERASE_OFFSET	S R	0x1		1 sec	
399:312	Reserved					
311:0	Reserved for Manufacturer					

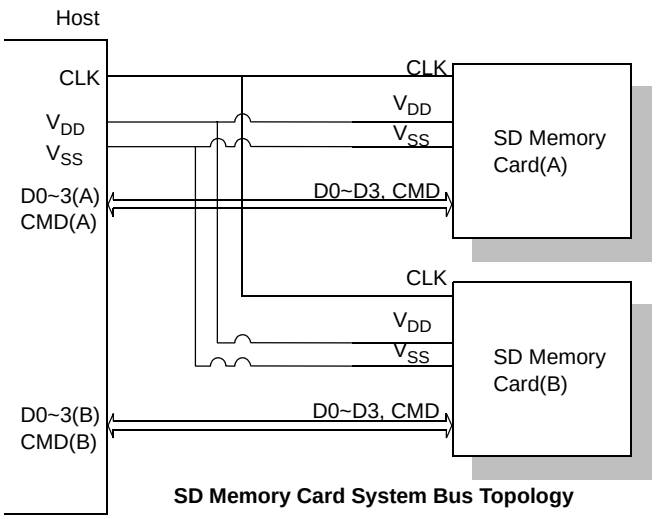
***Note:**
Speed Class that supports Class 10 shall not use the Pm value stored in the SD Status to calculate performance in any fragmented AU. Class 10 Performance is defined only for entirely free AUs

4.4 SPI Mode Card Registers

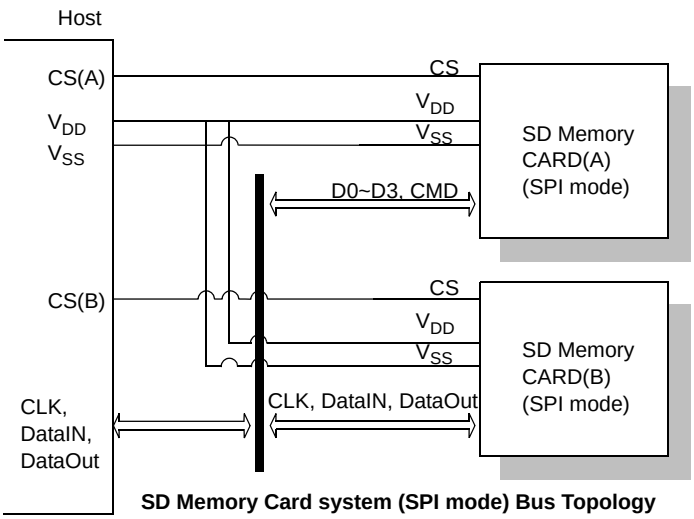
Unlike the SD Memory card protocol (where the register contents is sent as command response),reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by data block of 16 bytes suffixed with a 16-bit CRC.
The data timeout for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore, the standard response timeout value(N_{CR}) is used for read latency of the CSD register.

5.0 INTERFACE DESCRIPTION

5.1 SD/microSD SD mode Bus Topology / SD/microSD SPI Bus Topology



SD Memory Card System Bus Topology



SD Memory Card system (SPI mode) Bus Topology

The SD/microSD Memory Card system defines two alternative communication protocols: SD and SPI. The host system can choose either one of modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same communication mode. Common bus signals for multiple card slots are not recommended. A single SD bus should connect a single SD card. Where the host system supports a high-speed mode, a single SD bus shall be connected to a single SD card.

The SD/microSD bus includes the following signals:

- CMD : Bidirectional Command/Response signal
- DAT0 - DAT3 : 4 Bidirectional data signals
- CLK : Host to card clock signal
- V_{DD}, V_{SS1}, V_{SS2}: Power and ground signals

The SD/microSD Card bus has a single master (application), multiple slaves (cards), synchronous start topology (refer to Figure 5-2). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process, commands are sent to each card individualy, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simplify the handling of the card stack, after initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

SD Bus allows dynamic configuration of the number of data lines. After power-up, be defalut, the SD/microSD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width(number of active data lines). This feature allows and easy trade off between hardware cost and system performance. Note that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.

The SPI compatible communication mode of the SD/microSD Memory Card is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.
The SPI standard defines the physical link only, and not complete data transfer protocol. The SD/microSD Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD mode which enables the wide bus option.

The SD/microSD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the SD/microSD Card SPI channel consists the following four signals:

- CS : Host to card Chip Select signal
- CLK : Host to card clock signal
- DataIN : Host to card data signal
- DataOut: Card to host data signal

Another SPI common characteristic is byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal .

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

5.2 Bus Protocol

5.2.1 SD Bus

For more details, refer to Section 3.6.1 of the SDA Physical Layer Specification, Version 3.00

5.2.2 SPI Bus

For more details, refer to Chapter 7 of the SDA Physical Layer Specificaation, Version 3.00

5.3 SD/microSD Card Pin Assignment

5.3.1 SD Card Pin Assignment

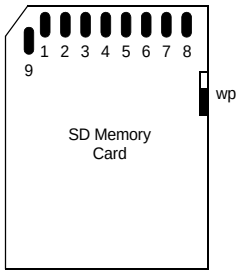


Figure 5-1. SD Memory Card shape and interface (top view)

The SD Memory Card has the form factor 24 mm x 32 mm x 2.1 mm or 24 mm x 32 mm x 1.4 mm.
Figure5-1 shows the general shape of the shape and interface contacts of the SD Memory Card. The detailed physical dimensions and mechanical description are given in section 5.4.
The following Table defines the card contacts:

[Table 5-1] : SD Memory Card Pad Assignment

Pin #	Name	Type[1]	Description	Name	Type	Description
SD Mode				SPI Mode		
1	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	V_{SS}	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	V_{DD}	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	V_{SS2}	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

5.3.2 microSD Card Assignment

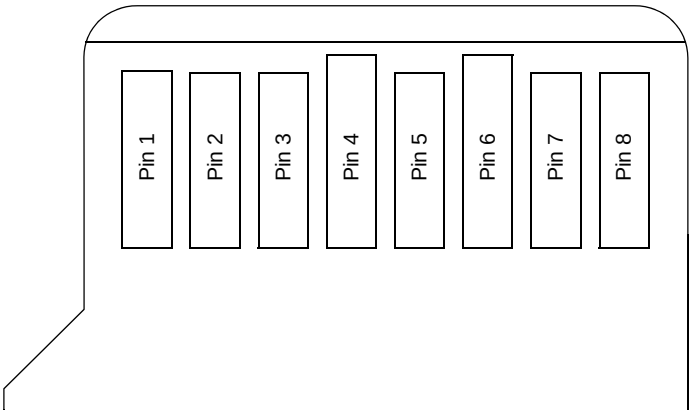


Figure 5-2. Contact Area

[Table 5-2] : microSD Contact Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	DAT2[2.5]	I/O/PP	Data Line [Bit 2]	RSV		Reserved
2	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[2.4]	I/O/PP	Data Line [Bit 1]	RSV[4]		

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers ;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42)
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

5.4 Mechanical Specification

This section describes the mechanical and electrical features, as well as SEC SD/microSD Card environmental reliability and durability specifications. For more details you can refer to Chapter 8 of SDA Physical Layer Specification, Version 2.00 and SDA ,microSD Card Addendum, Section 3.0 Mechanical Specification for microSD Memory Card.

5.4.1 Mechanical Form Factor of microSD

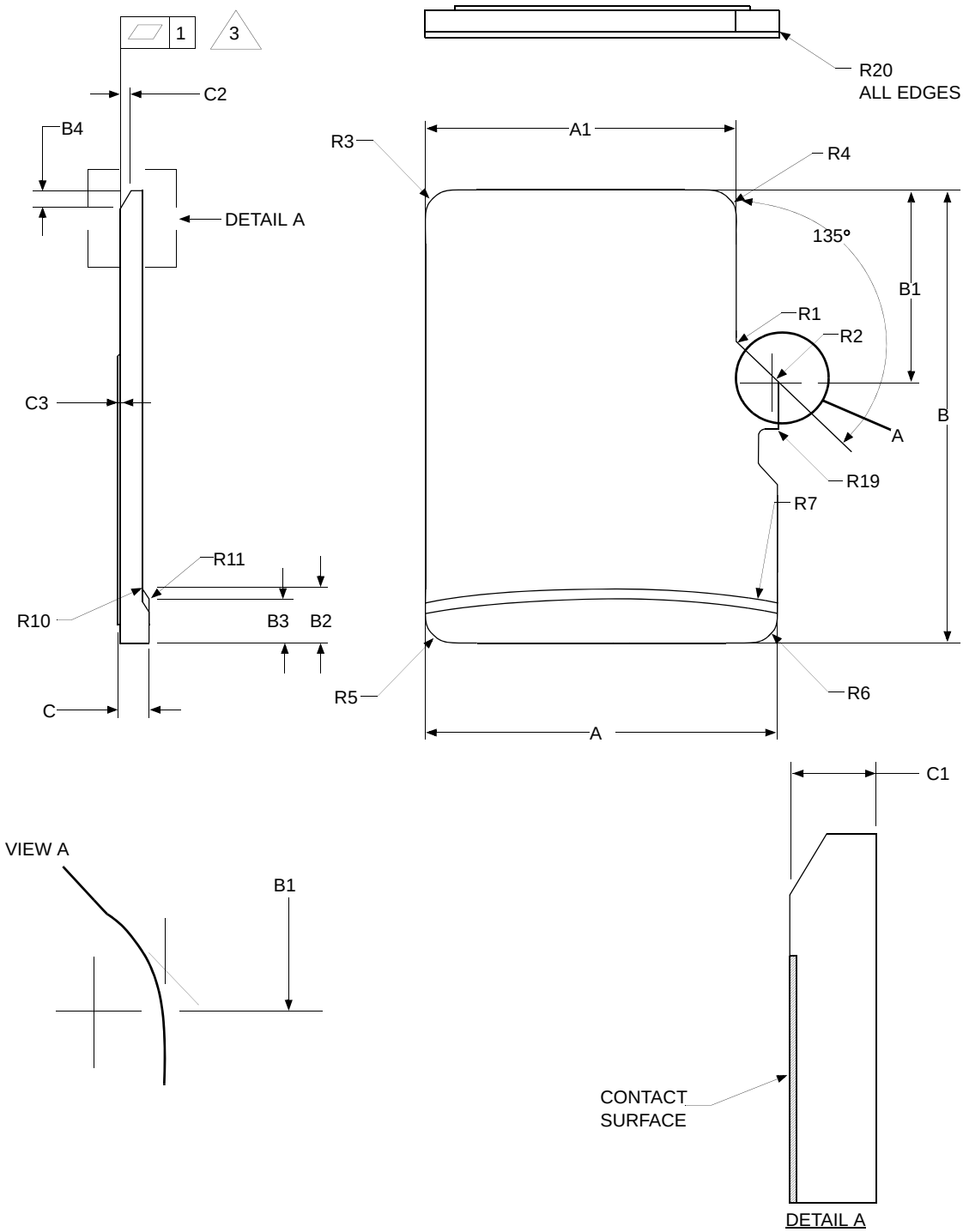


Figure 5-3. Mechanical Description: Top View

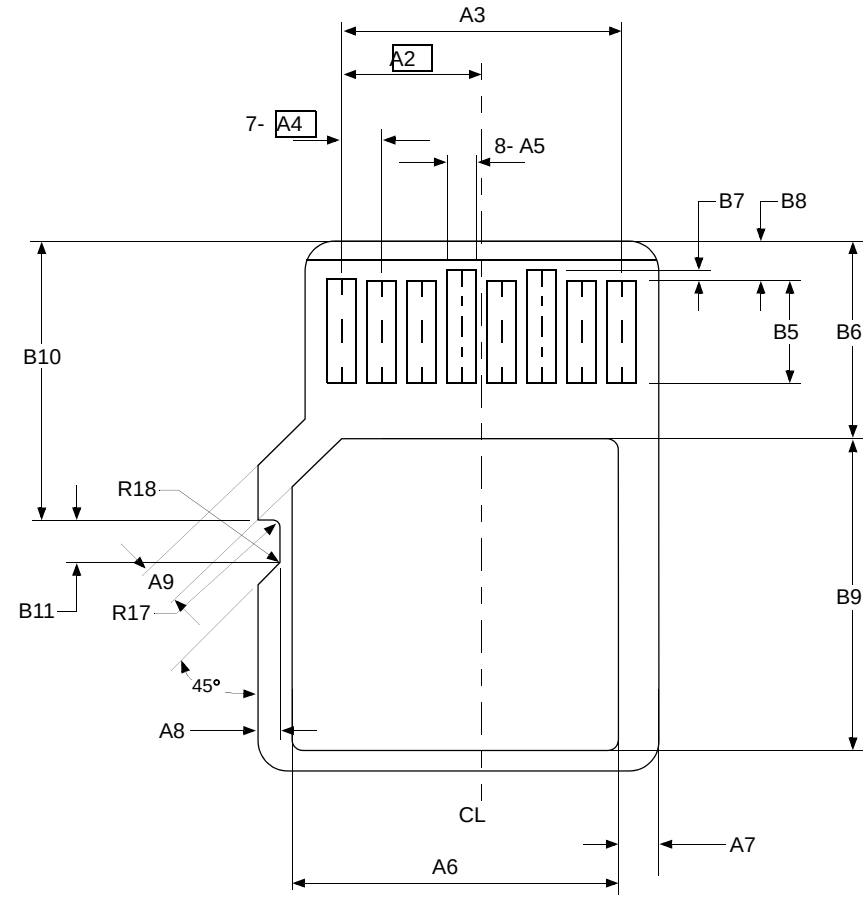


Figure 5-4. : Mechanical Description: Bottom View

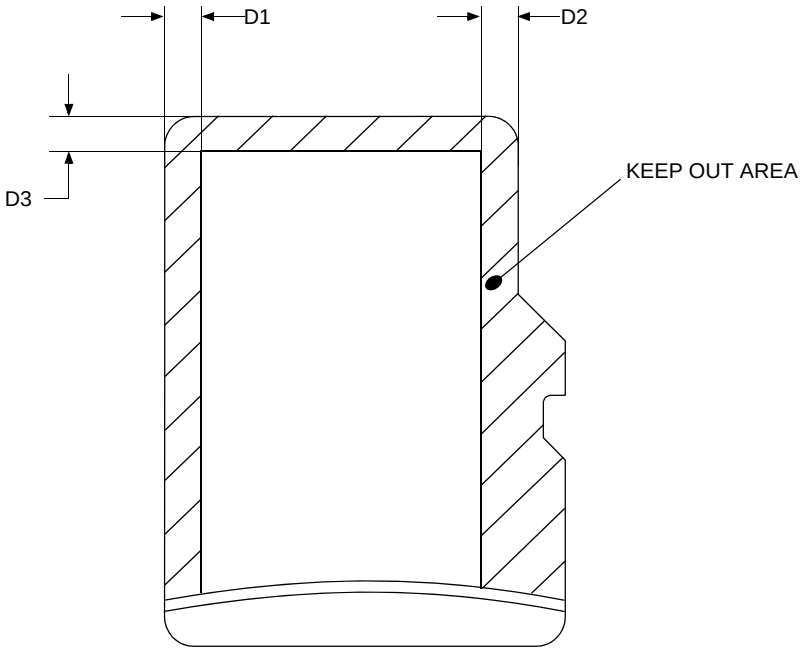


Figure 5-5. Mechanical Description: Keep Out Area

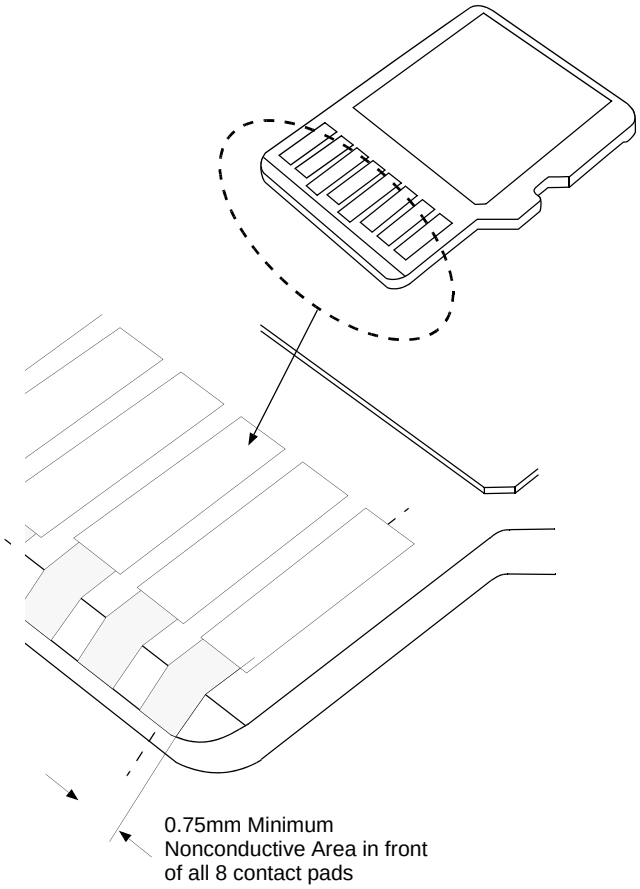


Figure 5-6. Nonconductive Area in Front of Contact Pad

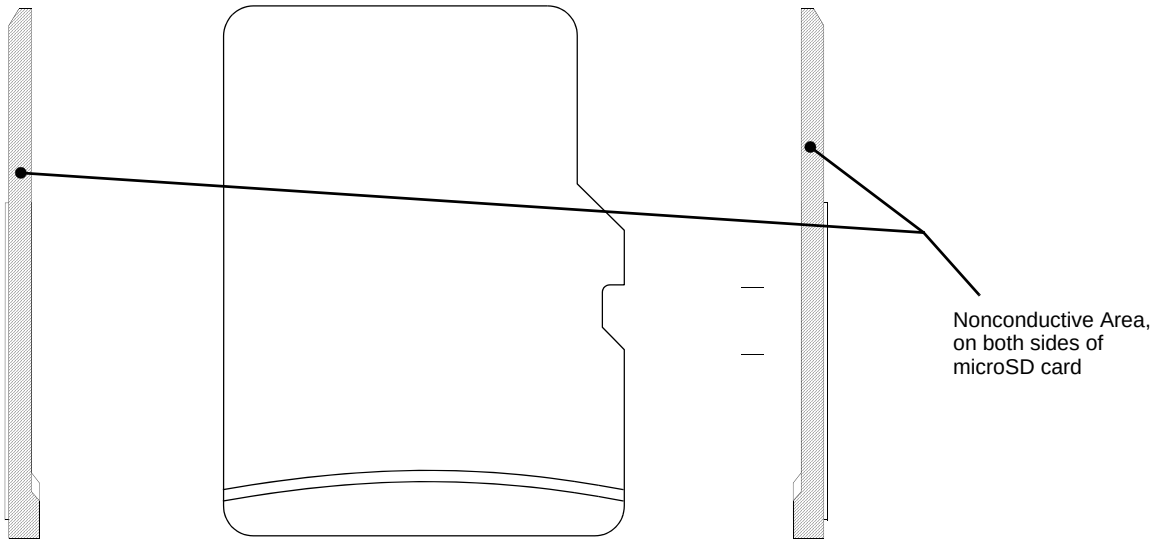


Figure 5-7. Nonconductive Area on Sides of Card

[Table 5-3] : microSD Package: Dimensions

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

NOTES:
1) DIMENSIONING AND TOLERTANCING PER ASME Y14.5M-1994.
2) DIMENSIONS ARE IN MILLIMETERS.
3) COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

5.4.2 Mechanical Form Factor of SD Card

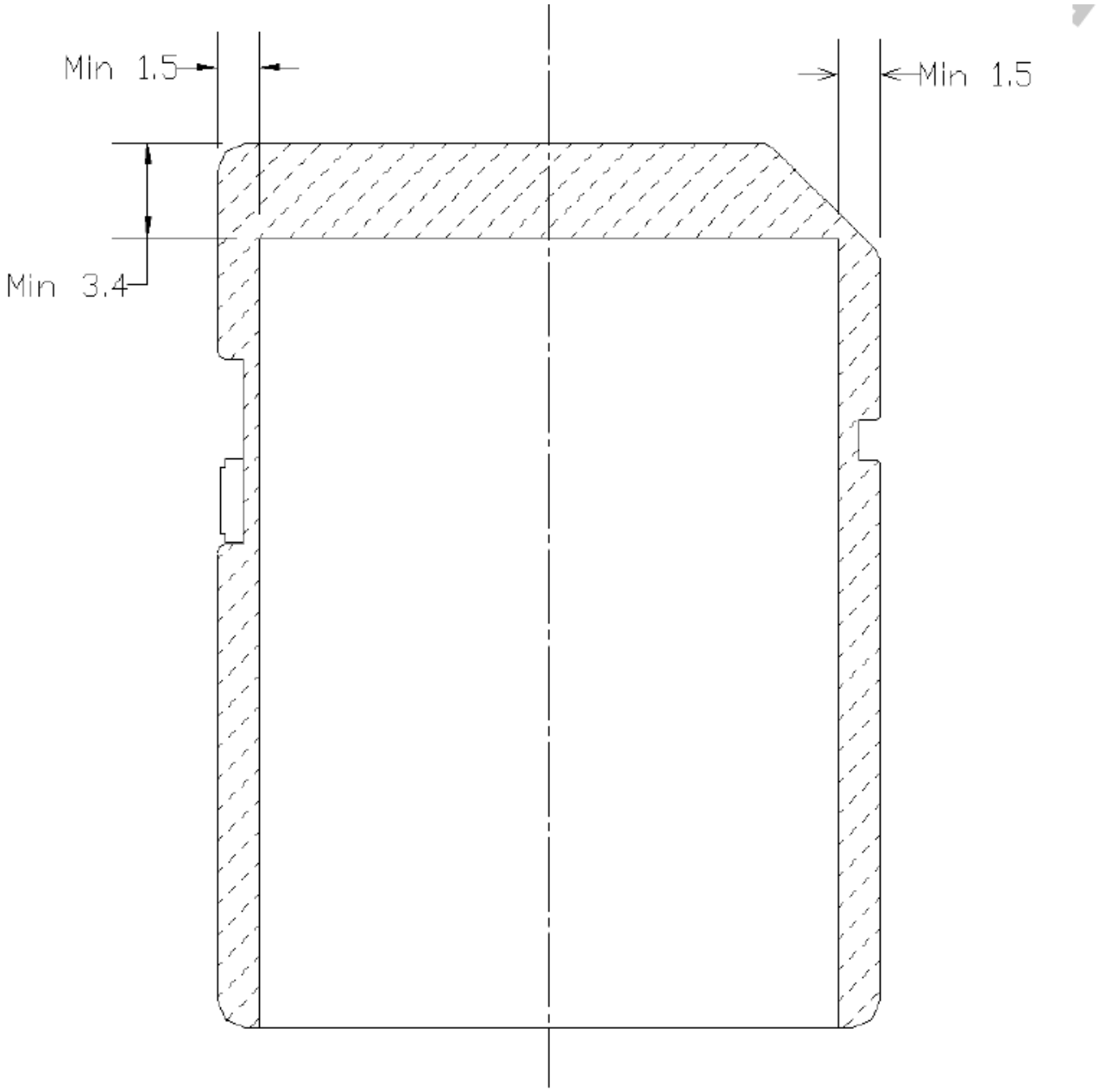


Figure 5-8. Mechanical Description: Top View - Keep Out Area

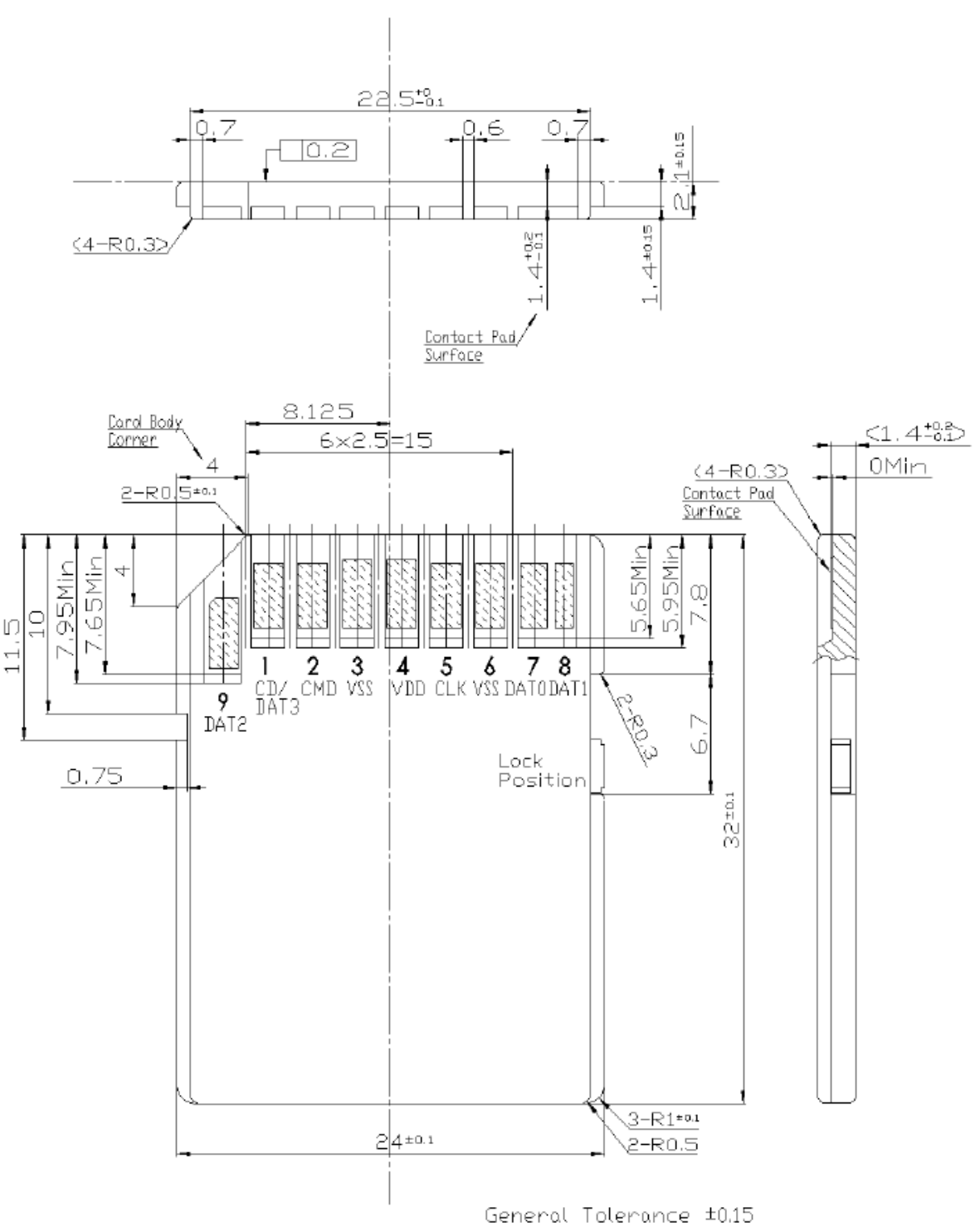


Figure 5-9. Mechanical Description

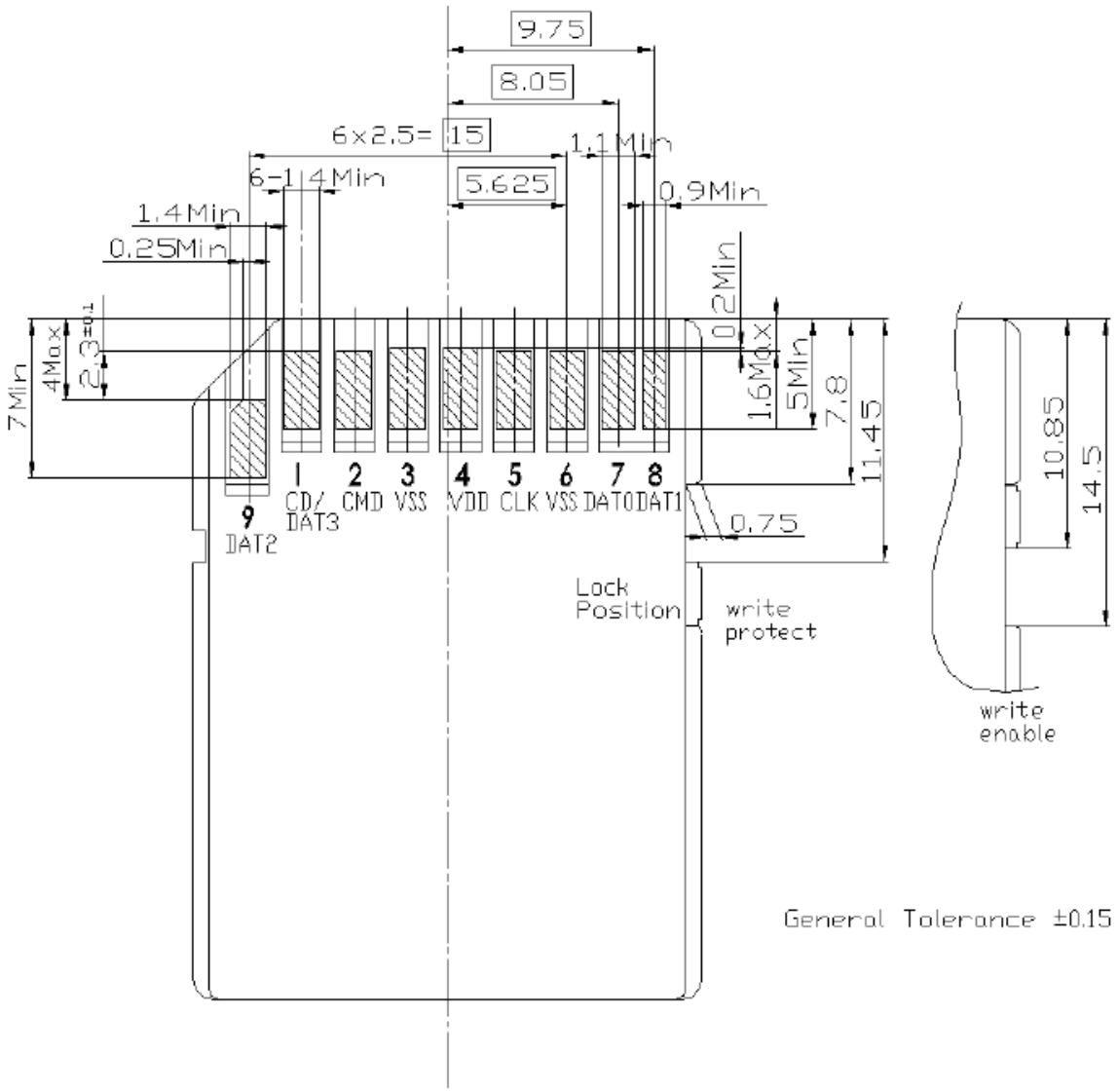


Figure 5-10. Mechanical Description: Bottom View

5.4.3 Electrical features, Environmental Reliability and Durability

SEC SD/microSD Card Electrical features, Environmental Reliabilities and Durabilities conform to SDA Physical Layer Specification Version 2.00, Section 8.1. For more details and informations of SEC SD/microSD Card Data, refer to Product Qualification Report.

5.5 Electrical Interface

The following sections provide valuable information about the electrical interface. See Chapter 6 of the SDA Physical Layer Specification, Version 3.00 for more detail information.

5.5.1 Power Up

The power-up of the SD/microSD Card bus is handled locally in each SD Card and in the host

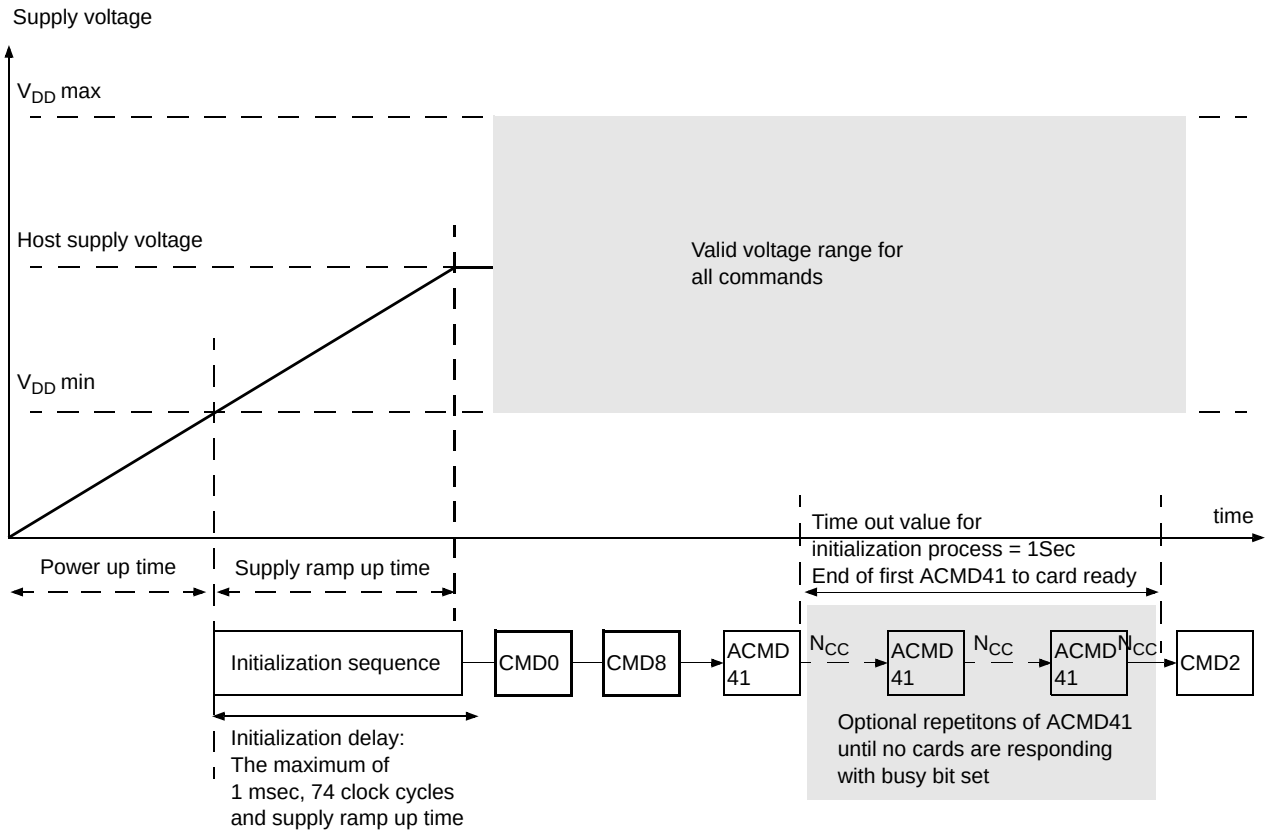


Figure 5-11. Power-up Diagram

.• Power up time is defined as voltage rising time from 0 volt to VDD(min.) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

• Supply ramp up time provides the time that the power is built up to the operating level (the host supply voltage) and the time to wait until the SD card can accept the first command,

• The host shall supply power to the card so that the voltage is reached to VDD(min.) within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

• After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the *idle state*. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

• CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

• ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

5.5.2 Reset Level Power Up

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

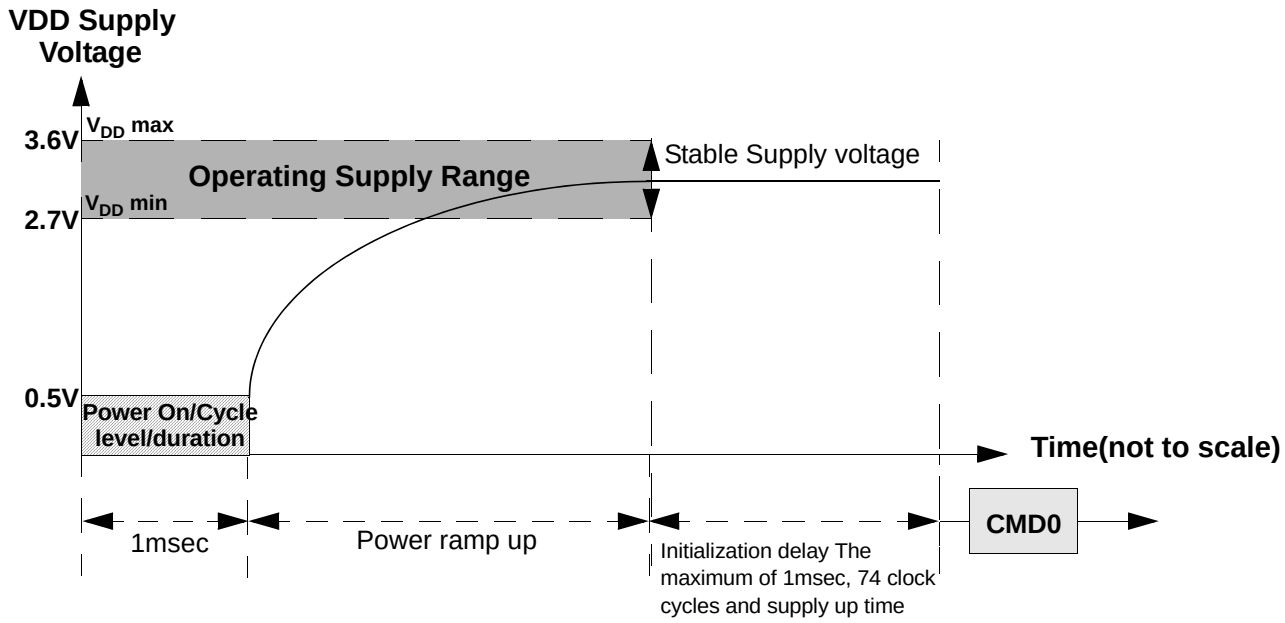


Figure 5-12. change of Figure for power up

• To assure a reliable SD Card hard reset of Power On and Power Cycle, Voltage level shall be below 0.5V and Time duration shall be at least 1ms.

• The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:
(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7~3.6V power supply.

5.5.3 Power Down and Power Cycle

• When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

• If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

5.5.4 Bus Operating Conditions for 3.3V Signaling

SPI Mode bus operating conditions are identical to SD Card mode bus operating conditions.

5.5.4.1 Threshold Level for High Voltage Range

[Table 5-4] : Threshold Level for High Voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25 *V_{DD}	V	
Power Up Time	=		250	ms	From 0V to $V_{DD\ min}$

5.5.4.2 Bus Signal Line Load

The total capacitance of the SD Memory Card bus is the sum of the bus host capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:

Total bus capacitance = C_{HOST} + C_{BUS} + N * C_{CARD}

Where N is the number of connected cards.

[Table 5-5] : Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KOhm	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30 pF
Capacitance of the card for each siginal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 20 MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KOhm	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To Prevent inrush current

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only because they are connected separately to the SD Memory Card host.
Host should consider total bus capacitance for each signal as the sum of C_{HOST}, C_{BUS}, and C_{CARD}, these parameters are defined by per signal. The host can determine C_{HOST} and C_{BUS} so that total bus capacitance is less than the card estimated capacitance load (C_L=40 pF). The SD Memory Card guarantees its bus timing when total bus capacitance is less than maximum value of C_L (40 pF). To limit inrush current caused by host insertion, card maximum capacitance between VDD - VSS is defined as 5uF. To support host hot insertion, the host should consider decoupling capacitor connected to power line. As SD/microSD card Cc is 5uF(Max.), 45uF(min.) is recommended for Decoupling capacitor. For more details, please refer to Appendix E of the SDA Physical Layer Specification 3.00.

5.5.5 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

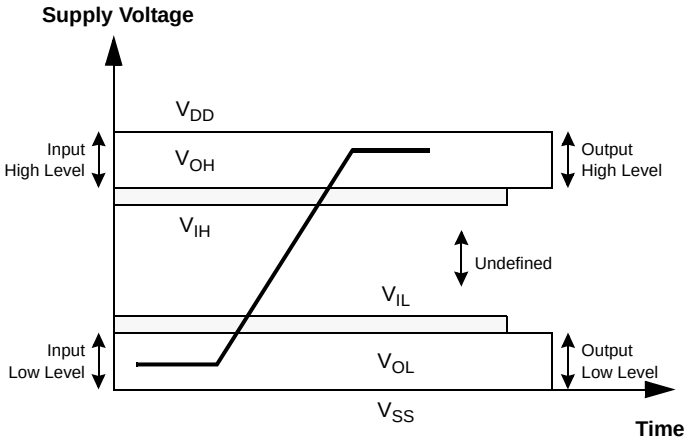


Figure 5-13. Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 5-2 for any VDD of the allowed voltage range.

5.5.6 Bus Timing (Default Mode)

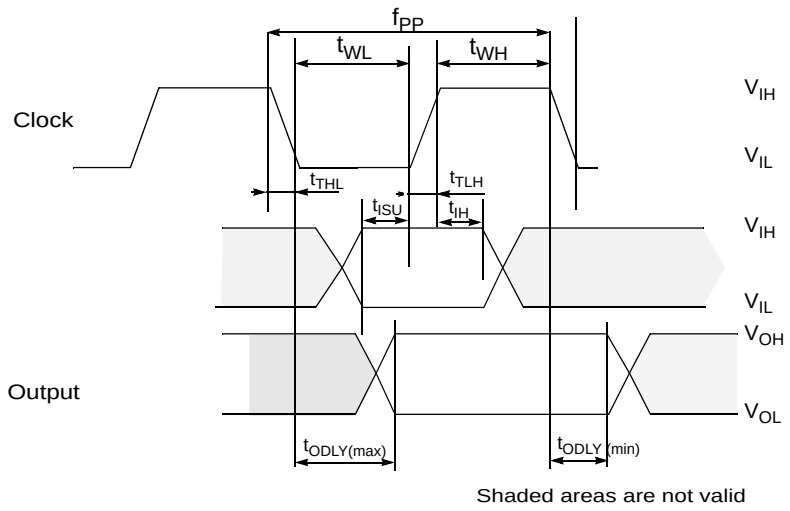


Figure 5-14. Timing diagram data input/output referenced to clock (Default)

[Table 5-6] : Bus Timing - Parameter Values (Default)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{CARD} <= 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$ / 100	400	kHz	C_{CARD} <= 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} <= 10 pF (1 card's)
Clock high time	t_{WH}	10		ns	C_{CARD} <= 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} <= 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} <= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} <= 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD} <= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L <= 40 pF (1 card)
Output delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L<= 40 pF (1 card)

(1) OHz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required

5.5.7 Bus Timing (High-speed Mode)

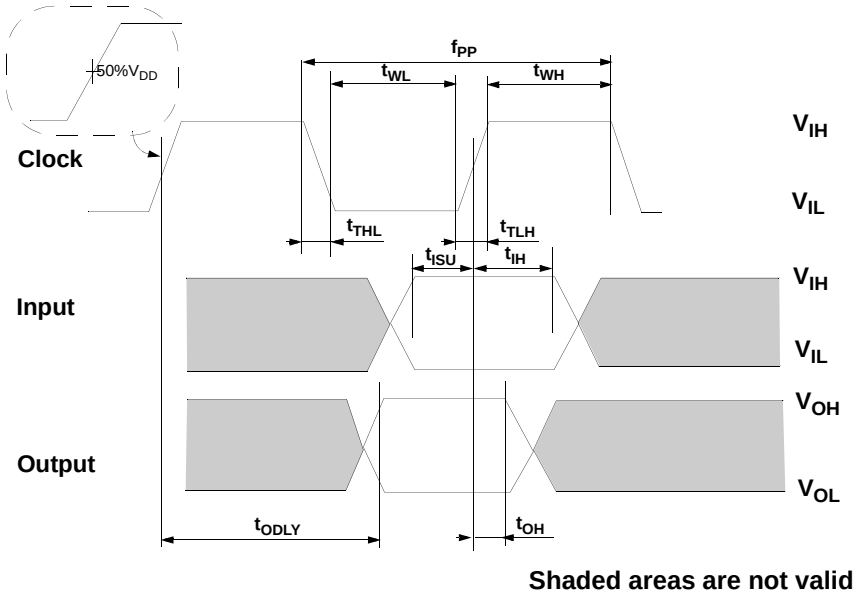


Figure 5-15. Timing Diagram data Input/Output Refrenced to Clock (High-Speed)

[Table 5-7] : Bus Timing - Parameter Values (High-Speed)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} <= 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} <= 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} <= 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} <= 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} <= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} <= 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} <= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L <= 40 pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L <= 15 pF (1 card)
Total Systme capacitance for each line[1]	C_L		40	pF	1 card

1) In order to satisfy severe timing, host shall drive only one card.

6.0 SD/MICROSD CARD FUNCTIONAL DESCRIPTION

6.1 General

SEC SD/microSD Card Functional Description contained in this chapter; Section 6.2~6.14; basically, comfort to SDA Physical Layer Specification, Version 3.00. See Chapter 4 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide.

6.2 Card Identification Mode

While in Card Identification mode the host resets all the cards that are in card identification mode, validates operation voltge range, identifies cards and asks them to publish Relative Card Address(RCA). This operation is done to each card separately on its own CMD line. Refer to Section 4.2 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide*

*Note : The products on this specification does not support UHS-1 mode. For correct identification flow, please refer to Section 4.2 of the SDA Physical Layer Specification, Version 2.00.

6.3 Clock Control

The SD/microSD Memory Card bus clock signal can be used by the host to change the cards to energy saving mode or to control the data flow(to avoid under-run or over-run conditions) on the bus. Refer to Section 4.4 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide

6.4 Cyclic Redundancy Code

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block, per data line, is generated. The CRC is generated and checked as described in the Section 4.5 of the SDA Physical Layer Specification, Version 3.0

6.5 Command

There are four kinds of commands defined to control the SD Card:

* Broadcast commands (bc), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated then each card will accept it separately on his turn.
* Broadcast commands with response (bcr) - response from all cards simultaneously. Since there is no Open Drain mode in SD Card, this type of command is used only if all the CMD lines are separated. The command will be accepted and responded to by every card seperately.
* Addressed (point-to-point) commands (ac) - no data transfer on DAT lines
* Addressed (point-to-point) data transfer commands (adtc), data transfer on DAT lines

All commands and responses are sent over the CMD line of the SD Card bus. The command transmission always starts with the left bit of the bitstring corresponding to the command code word. For more details, refer to the Section 4.7 of the SDA Physical Layer Specification, Version 3.0.

Note: Limited Vendor CMD information, only for certain customer and application, can be provided under appropriate purpose of usage.

6.6 Memory Array Partitioning

The basic unit of data transfer to/from the SD Card is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

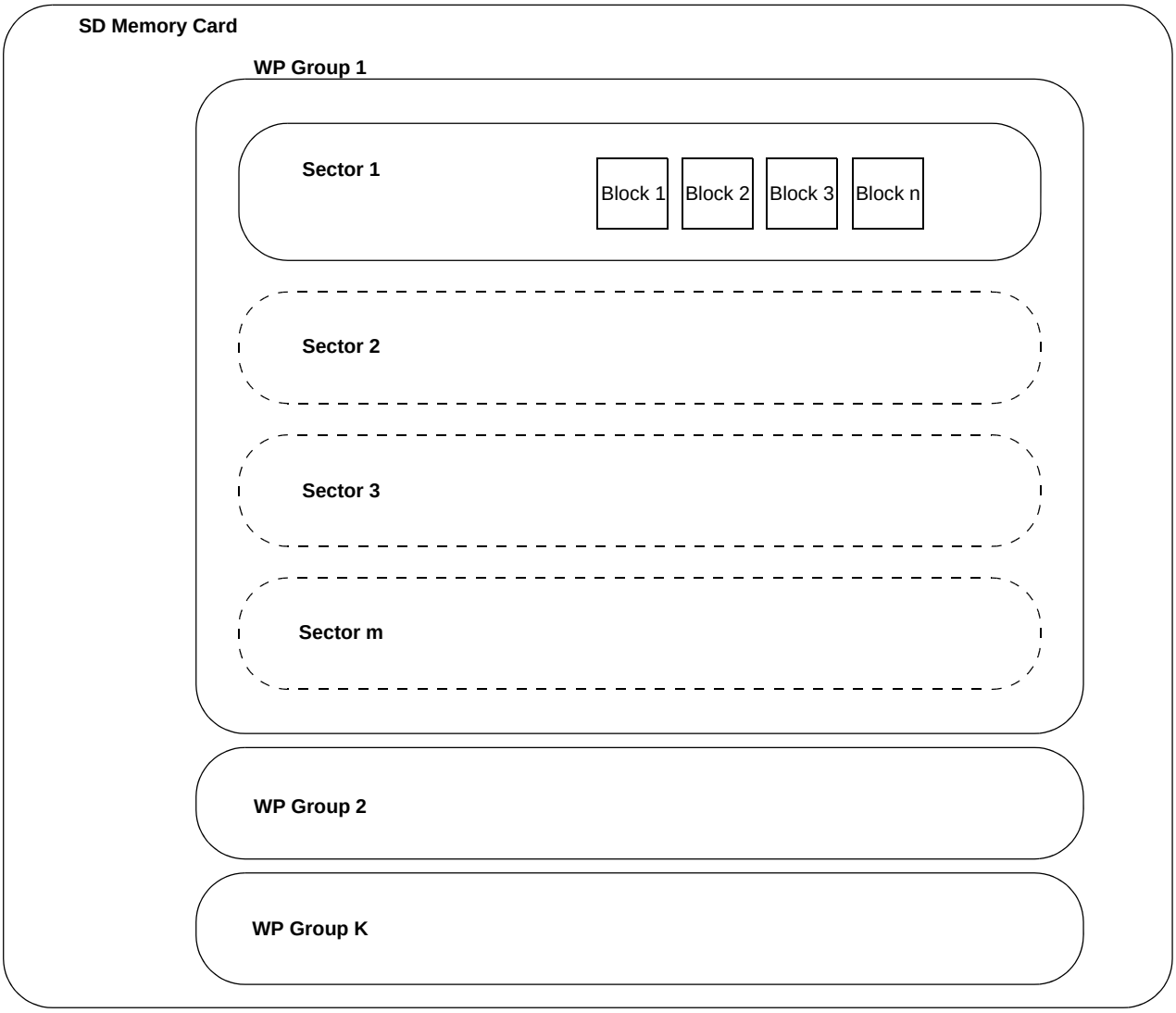


Figure 6-1: Write Protection Hierarchy

For block oriented commands, the following definition is used:

- Block: is the unit that is related to the block oriented read and write commands. Its size is the number of bytes that will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.
- For devices that have erasable memory cells, special erase commands are defined. The granularity of the erasable units is in general not the same as for the block oriented commands:
- Sector: is the unit that is related to the erase commands. Its size is the number of blocks that will be erased in one portion. The size of a sector is fixed for each device. The information about the sector size (in blocks) is stored in the CSD. Note that if the card specifies AU size, sector size should be ignored.
- AU (Allocation Unit): is a physical boundary of the card and consists of one or more blocks and its size depends on each card. The maximum AU size is defined for memory capacity. Furthermore AU is the minimal unit in which the card guarantees its performance for devices which complies with Speed Class Specification. The information about the size and the Speed Class are stored in the SD Status. AU is also used to calculate the erase timeout.
- WP-Group: is the minimal unit that may have individual write protection for devices which support write-protected group. Its size is the number of groups that will be write-protected by one bit. The size of a WP-group is fixed for each device. The information about the size is stored in the CSD.

The High Capacity SD Memory Card does not support the write protect group command.

6.7 Timings

Refer to Section 4.12 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide*

*Note : The products on this specification does not support UHS-1 mode.

6.8 Speed Class Specification

Refer to Section 4.13 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide*

*Note : The products on this specification does not support UHS-1 mode.

6.9 Erase Timeout Calculation

Refer to Section 4.14 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide*

*Note : The products on this specification does not support UHS-1 mode.