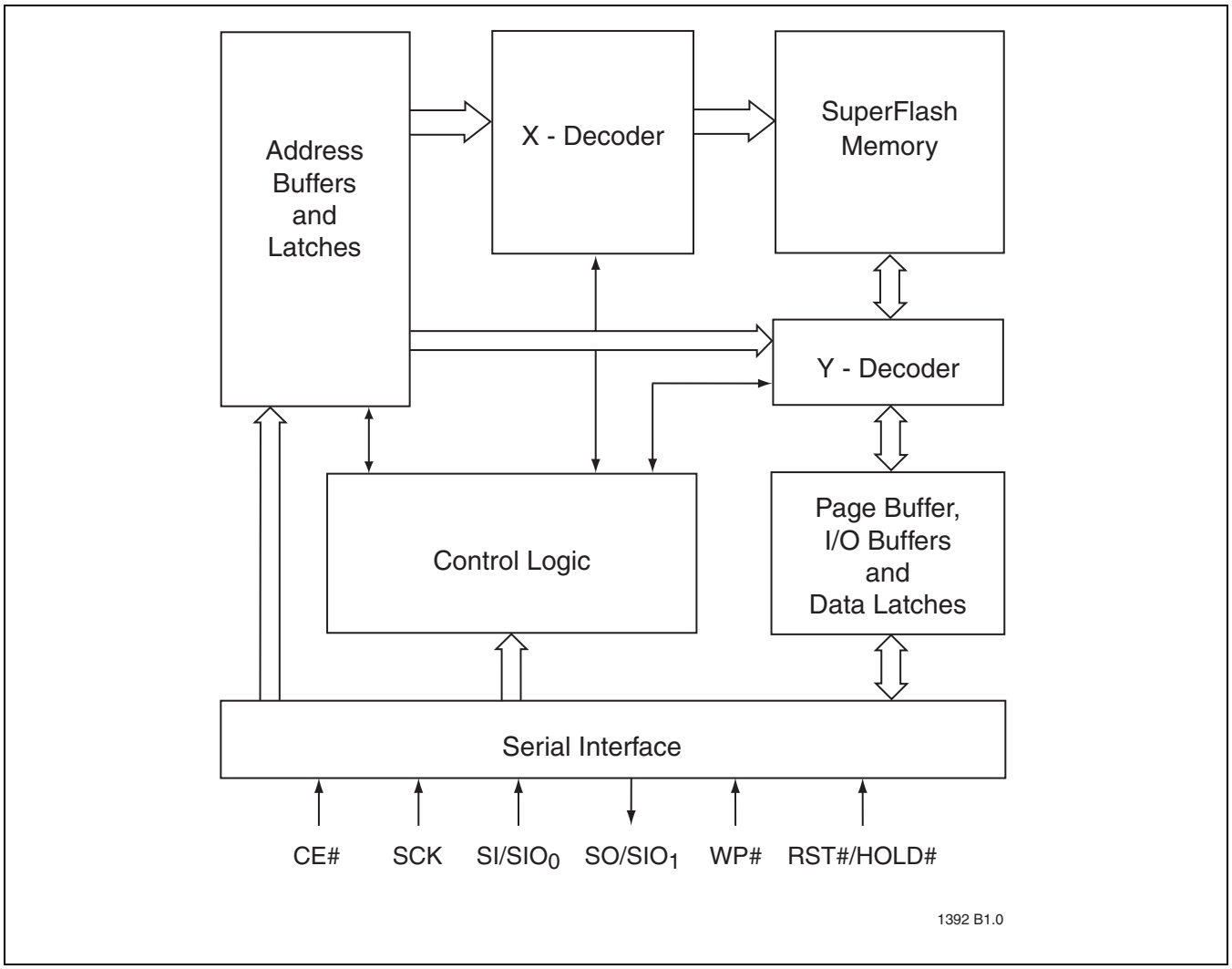

FIGURE 1: Functional Block Diagram

PIN DESCRIPTION

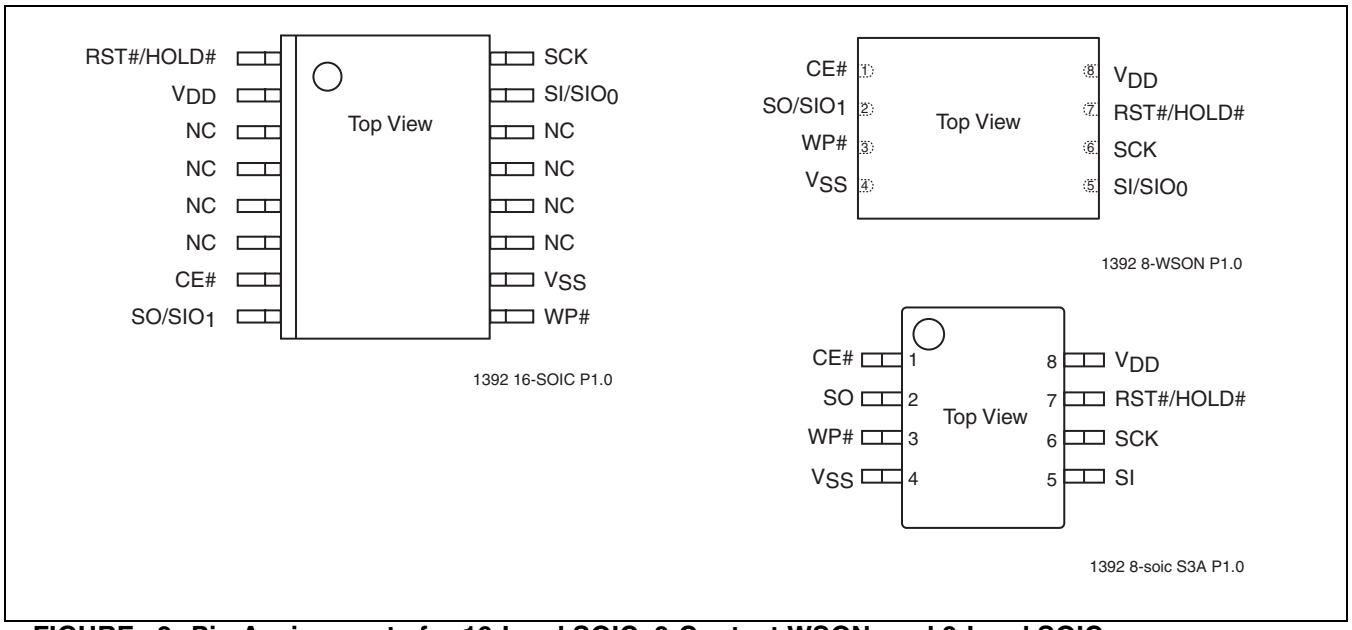

FIGURE 2: Pin Assignments for 16-Lead SOIC, 8-Contact WSON, and 8-Lead SOIC

TABLE 1: Pin Description

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing of the serial interface. Commands, addresses, or input data are latched on the rising edge of the clock input, while output data is shifted out on the falling edge of the clock input.
SI	Serial Data Input	To transfer commands, addresses, or data serially into the device. Inputs are latched on the rising edge of the serial clock.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.
SIO[0:1]	Serial Data Input/ Output for Dual I/O Mode	To transfer commands, addresses, or data serially into the device, or data out of the device. Inputs are latched on the rising edge of the serial clock. Data is shifted out on the falling edge of the serial clock. These pins are for Dual I/O mode.
CE#	Chip Enable	The device is enabled by a high to low transition on CE#. CE# must remain low for the duration of any command sequence.
WP#	Write Protect	The Write Protect (WP#) pin is used to enable/disable BPL bit in the status register.
RST#/HOLD#	Reset	To reset the operation of the device and the internal logic. The device powers on with RST# pin functionality as default.
	Hold	To temporarily stop serial communication with SPI Flash memory while device is selected. This is selected by an instruction sequence. See “Reset/Hold Mode” page 5 for details.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	

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MEMORY ORGANIZATION

The PCT25VF064C SuperFlash memory array is organized in uniform 4 KByte erasable sectors with 32 KByte overlay blocks and 64 KByte overlay erasable blocks.

DEVICE OPERATION

The PCT25VF064C is accessed through the SPI (Serial Peripheral Interface) bus compatible protocol. The SPI bus consists of four control lines; Chip Enable (CE#) is used to select the device, and data is accessed through the Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK).

The PCT25VF064C supports both Mode 0 (0,0) and Mode 3 (1,1) of SPI bus operations. The difference between the two modes, as shown in Figure 3, is the state of the SCK signal when the bus master is in Stand-by mode and no data is being transferred. The SCK signal is low for Mode 0 and SCK signal is high for Mode 3. For both modes, the Serial Data In (SI) is sampled at the rising edge of the SCK clock signal and the Serial Data Output (SO) is driven after the falling edge of the SCK clock signal.

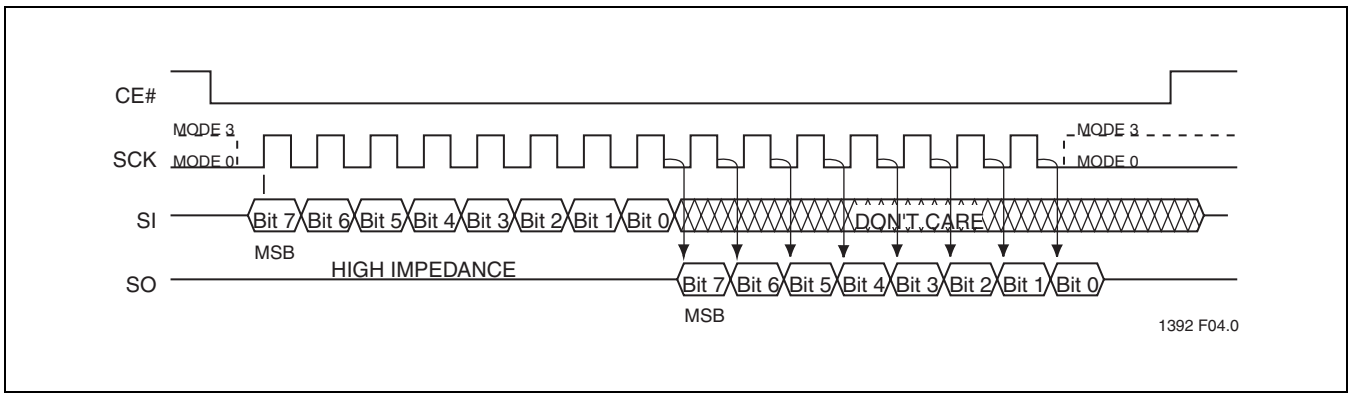

FIGURE 3: SPI Protocol

Reset/Hold Mode

The RST#/HOLD# pin provides either a hardware reset or a hold pin. From power-on, the RST#/HOLD# pin defaults as a hardware reset pin (RST#). The Hold mode for this pin is a user selected option where an EHLD instruction enables the Hold mode. Once selected as a hold pin (HOLD#), the RST#/HOLD# pin will be configured as a HOLD# pin, and goes back to RST# pin only after a power-off and power-on sequence.

Reset

If the RST#/HOLD# pin is used as a reset pin, RST# pin provides a hardware method for resetting the device. Driving the RST# pin high puts the device in normal operating mode. The RST# pin must be driven low for a minimum of T_{RST} time to reset the device. The SO pin is in high impedance state while the device is in reset. A successful reset will reset the status register to its power-up state (BPL, BUSY and WEL = 0; BP3, BP2, BP1, and BP0 = 1). See Table 2 for default power-up modes. A device reset during an active Program or Erase operation aborts the operation and data of the targeted address range may be corrupted or lost due to the aborted erase or program operation.

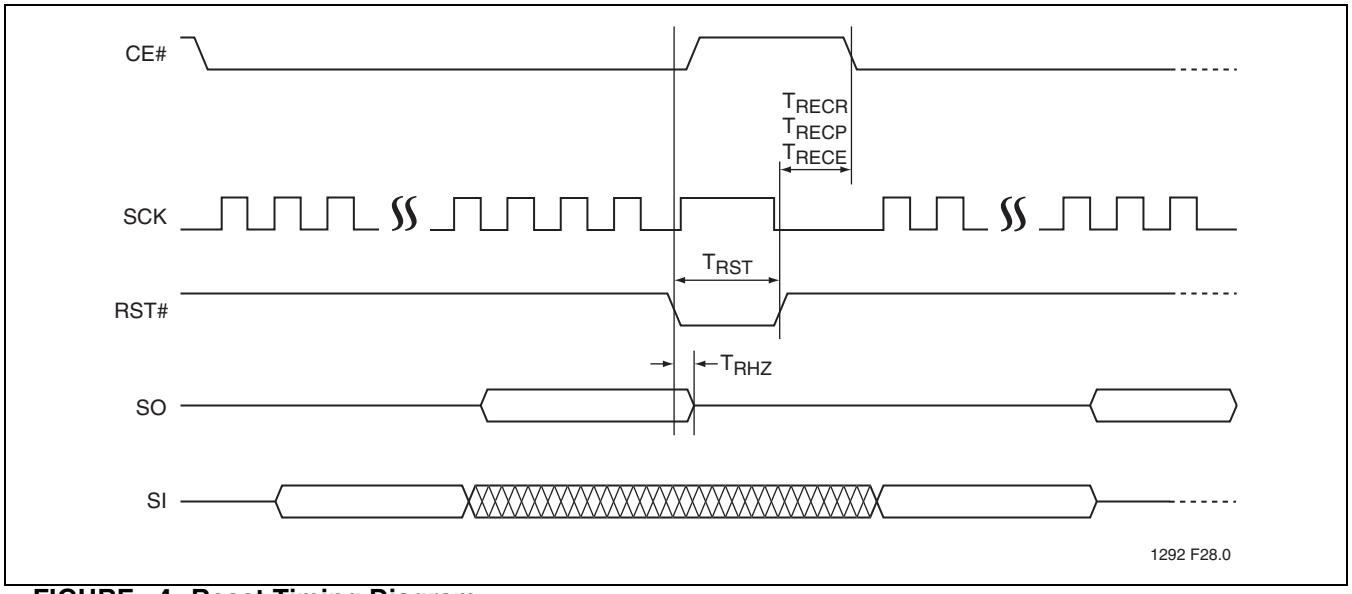

FIGURE 4: Reset Timing Diagram

TABLE 2: Reset Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{RST}	Reset Pulse Width	100		ns
T_{RHZ}	Reset to High-Z Output		105	ns
T_{RECR}	Reset Recovery from Read		100	ns
T_{RECP}	Reset Recovery from Program		10	µs
T_{RECE}	Reset Recovery from Erase		1	ms

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Hold Operation

The EHLD instruction enables the hold pin functionality of the RST#/HOLD# pin. Once converted to a hold pin, the RST#/HOLD# pin functions as a hold pin until the device is powered off and on. After the power cycle, the pin functionality returns as a reset pin (RST#) after the power on.

The HOLD# pin is used to pause a serial sequence using the SPI flash memory, but without resetting the clocking sequence. To activate the HOLD# mode, CE# must be in active low state. The HOLD# mode begins when the SCK active low state coincides with the falling edge of the HOLD# signal. The HOLD mode ends when the HOLD# signal's rising edge coincides with the SCK active low state.

If the falling edge of the HOLD# signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state. Similarly, if the rising edge of the HOLD# signal does not coincide with the SCK active low state, then the device exits from Hold mode when the SCK next reaches the active low state. See Figure 5 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high-impedance state while SI and SCK can be V_{IL} or V_{IH}.

If CE# is driven high during a Hold condition, the device returns to Standby mode. As long as HOLD# signal is low, the memory remains in the Hold condition. To resume communication with the device, HOLD# must be driven active high, and CE# must be driven active low. See Figure 5 for Hold timing.

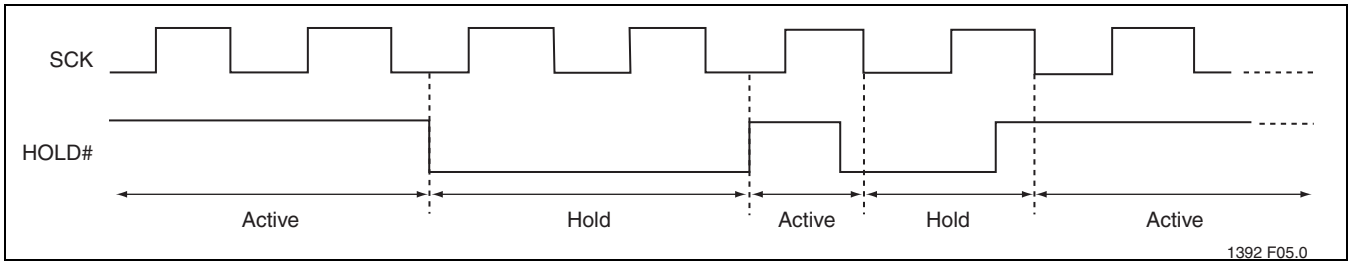

FIGURE 5: Hold Condition Waveform

Write Protection

PCT25VF064C provides software Write protection. The Write Protect pin (WP#) enables or disables the lock-down function of the status register. The Block-Protection bits (BP3, BP2, BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 5 for the Block-Protection description.

Write Protect Pin (WP#)

The Write Protect (WP#) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When WP# is driven low, the execution of the Write-Status-Register (WRSR) instruction is determined by the value of the BPL bit (see Table 3). When WP# is high, the lock-down function of the BPL bit is disabled.

TABLE 3: Conditions to execute Write-Status-Register (WRSR) Instruction

WP#	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

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Security ID

PCT25VF064C offers a 256-bit Security ID (Sec ID) feature. The Security ID space is divided into two parts – one factory-programmed, 64-bit segment and one user-programmable 192-bit segment. The factory-programmed segment is programmed at SST with a unique number and cannot be changed. The user-programmable segment is left unprogrammed for the customer to program as desired.

Use the Program SID command to program the Security ID using the address shown in Table 7. Once programmed, the Security ID can be locked using the Lockout SID command. This prevents any future write to the Security ID.

The factory-programmed portion of the Security ID can never be programmed, and none of the Security ID can be erased.

Status Register

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the Memory Write protection. During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. Table 4 describes the function of each bit in the software status register.

TABLE 4: Status Register

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 5)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 5)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 5)	1	R/W
5	BP3	Indicate current level of block write protection (See Table 5)	1	R/W
6	SEC[1]	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0[1]	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are readable/writable	0	R/W

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1. The Security ID status will always be ‘1’ at power-up after a successful execution of the Lockout SID instruction; otherwise, the default at power up is ‘0’.

Busy

The Busy bit determines whether there is an internal Erase or Program operation in progress. A ‘1’ for the Busy bit indicates the device is busy with an operation in progress. A ‘0’ indicates the device is ready for the next valid operation.

Write Enable Latch (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If the Write-Enable-Latch bit is set to ‘1’, it indicates the device is Write enabled. If the bit is set to ‘0’ (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/Erase) commands. The Write-Enable-Latch bit is automatically reset under the following conditions:

- Power-up
- Write-Disable (WRDI) instruction completion
- Write-Status Register instruction completion
- Page-Program instruction completion
- Dual-Input Page-Program instruction completion
- Sector-Erase instruction completion
- Block-Erase instruction completion
- Chip-Erase instruction completion
- Program SID instruction completion
- Lockout SID instruction completion

Block Protection (BP3,BP2, BP1, BP0)

The Block-Protection (BP3, BP2, BP1, BP0) bits define the size of the memory area, as shown in Table 5, to be software protected against any memory Write (Program or Erase) operation. The Write-Status-Register (WRSR) instruction is used to program the BP3, BP2, BP1 and BP0 bits as long as WP# is high or the Block-Protect-Lock (BPL) bit is 0. Chip-Erase can only be executed if Block-Protection bits are all 0. After power-up, BP3, BP2, BP1 and BP0 are set to the defaults specified in Table 5.

Block Protection Lock-Down (BPL)

WP# pin driven low (V_{IL}), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP3, BP2, BP1, and BP0 bits. When the WP# pin is driven high (V_{IH}), the BPL bit has no effect and its value is "Don't Care". After power-up, the BPL bit is reset to 0.

Security ID Status (SEC)

The Security ID Status (SEC) bit indicates when the Security ID space is locked to prevent a Write command. The SEC is '1' after the host issues a Lockout SID command. Once the host issues a Lockout SID command, the SEC bit can never be reset to '0.'

TABLE 5: Software Status Register Block Protection FOR PCT25VF064C

	Status Register Bit[1]				Protected Memory Address
Protection Level	**BP3**	**BP2**	**BP1**	**BP0**	**64 Mbit**
None	0	0	0	0	None
Upper 1/128	0	0	0	1	7F0000H-7FFFFFH
Upper 1/64	0	0	1	0	7E0000H-7FFFFFH
Upper 1/32	0	0	1	1	7C0000H-7FFFFFH
Upper 1/16	0	1	0	0	780000H-7FFFFFH
Upper 1/8	0	1	0	1	700000H-7FFFFFH
Upper 1/4	0	1	1	0	600000H-7FFFFFH
Upper 1/2	0	1	1	1	400000H-7FFFFFH
All Blocks	1	0	0	0	000000H-7FFFFFH
All Blocks	1	0	0	1	000000H-7FFFFFH
All Blocks	1	0	1	0	000000H-7FFFFFH
All Blocks	1	0	1	1	000000H-7FFFFFH
All Blocks	1	1	0	0	000000H-7FFFFFH
All Blocks	1	1	0	1	000000H-7FFFFFH
All Blocks	1	1	1	0	000000H-7FFFFFH
All Blocks	1	1	1	1	000000H-7FFFFFH

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1. Default at power-up for BP3, BP2, BP1, and BP0 is '1111'. (All Blocks Protected)

INSTRUCTIONS

Instructions are used to read, write (Erase and Program), and configure the PCT25VF064C. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. The Write-Enable (WREN) instruction must be executed prior any Page-Program, Dual-Input Page-Program, Sector-Erase, Block-Erase, Write-Status-Register, Chip-Erase, Program SID, or Lockout SID instructions. The complete list of instructions is provided in Table 6.

All instructions are synchronized off a high to low transition of CE#. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. CE# must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read-ID, and Read-Status-Register instructions). Any low to high transition on CE#, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to standby mode. Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

TABLE 6: Device Operation Instructions

Instruction	Description	Op Code Cycle[1]	Address Cycle(s)[2]	Dummy Cycle(s)	Data Cycle(s)
Read	Read Memory	0000 0011b (03H)	3	0	1 to ∞
Fast-Read Dual I/O	Read Memory with Dual Address Input and Data Output	1011 1011b (BBH)	3[3]	1[3]	1 to ∞[3]
Fast-Read Dual-Output	Read Memory with Dual Output	0011 1011b (3BH)	3	1	1 to ∞[3]
High-Speed Read	Read Memory at Higher Speed	0000 1011b (0BH)	3	1	1 to ∞
Sector-Erase[4]	Erase 4 KByte of memory array	0010 0000b (20H)	3	0	0
32 KByte Block-Erase[5]	Erase 32KByte block of memory array	0101 0010b (52H)	3	0	0
64 KByte Block-Erase[6]	Erase 64 KByte block of memory array	1101 1000b (D8H)	3	0	0
Chip-Erase	Erase Full Memory Array	0110 0000b (60H) or 1100 0111b (C7H)	0	0	0
Page-Program	To Program 1 to 256 Data Bytes	0000 0010b (02H)	3	0	1 to 256
Dual-Input Page-Program	To Program 1 to 256 Data Bytes	1010 0010b (A2H)	3	0	1 to 128[3]
RDSR[7]	Read-Status-Register	0000 0101b (05H)	0	0	1 to ∞
EWSR	Enable-Write-Status-Register	0101 0000b (50H)	0	0	0
WRSR	Write-Status-Register	0000 0001b (01H)	0	0	1
WREN	Write-Enable	0000 0110b (06H)	0	0	0
WRDI	Write-Disable	0000 0100b (04H)	0	0	0
RDID[8]	Read-ID	1001 0000b (90H) or 1010 1011b (ABH)	3	0	1 to ∞
JEDEC-ID	JEDEC ID Read	1001 1111b (9FH)	0	0	3 to ∞
EHLD	Enable HOLD# pin functionality of the RST#/HOLD# pin	1010 1010b (AAH)	0	0	0
Read SID	Read Security ID	1000 1000b (88H)	1	1	1 to 32
Program SID[9]	Program User Security ID area	1010 0101b (A5H)	1	0	1 to 24
Lockout SID[9]	Lockout Security ID Programming	1000 0101b (85H)	0	0	0

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1. One bus cycle is eight clock periods.
2. Address bits above the most significant bit can be either V_{IL} or V_{IH}.
3. One bus cycle is four clock periods (dual operation)
4. 4KByte Sector Erase addresses: use A_{MS}-A_{12}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.

5. 32KByte Block Erase addresses: use A_{MS}-A_{15}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
6. 64KByte Block Erase addresses: use A_{MS}-A_{16}, remaining addresses are don't care but must be set either at V_{IL} or V_{IH}.
7. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on CE#.
8. Manufacturer's ID is read with A_0 = 0, and Device ID is read with A_0 = 1. All other address bits are 00H. The Manufacturer's ID and device ID output stream is continuous until terminated by a low-to-high transition on CE#.
9. Requires a prior WREN command.

Read (33 MHz)

The Read instruction, 03H, supports up to 33 MHz Read. The device outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, once the data from address location 7FFFFFH has been read, the next output will be from address location 000000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits A_{23}-A_0. CE# must remain active low for the duration of the Read cycle. See Figure 6 for the Read sequence.

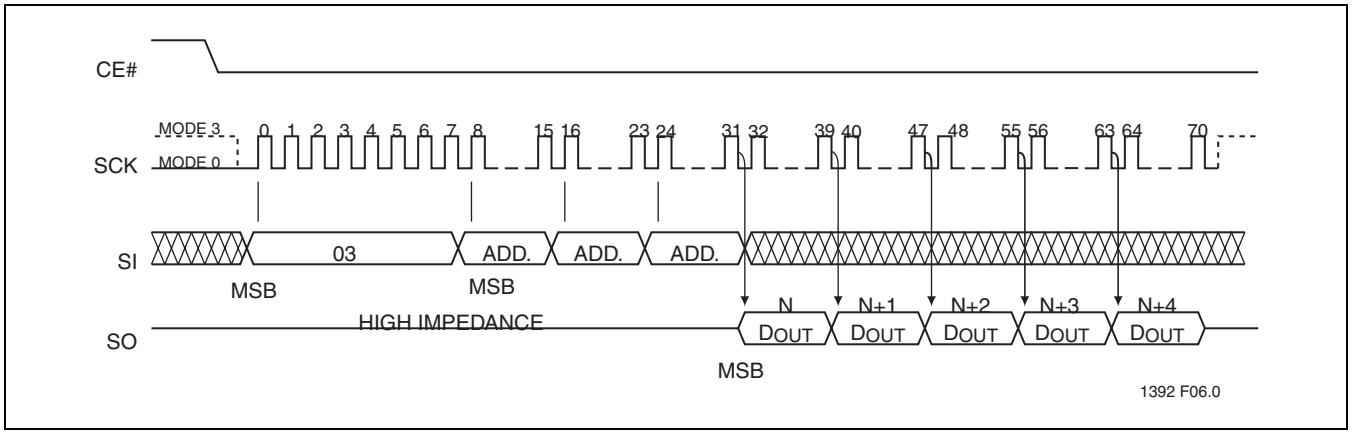

FIGURE 6: Read Sequence

High-Speed Read (80 MHz)

The High-Speed Read instruction supporting up to 80 MHz Read is initiated by executing an 8-bit command, 0BH, followed by address bits A_{23}-A_0 and a dummy byte. CE# must remain active low for the duration of the High-Speed Read cycle. See Figure 7 for the High-Speed Read sequence.

Following a dummy cycle, the High-Speed Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space. For example, once the data from address location 7FFFFFH is read, the next output is from address location 000000H.

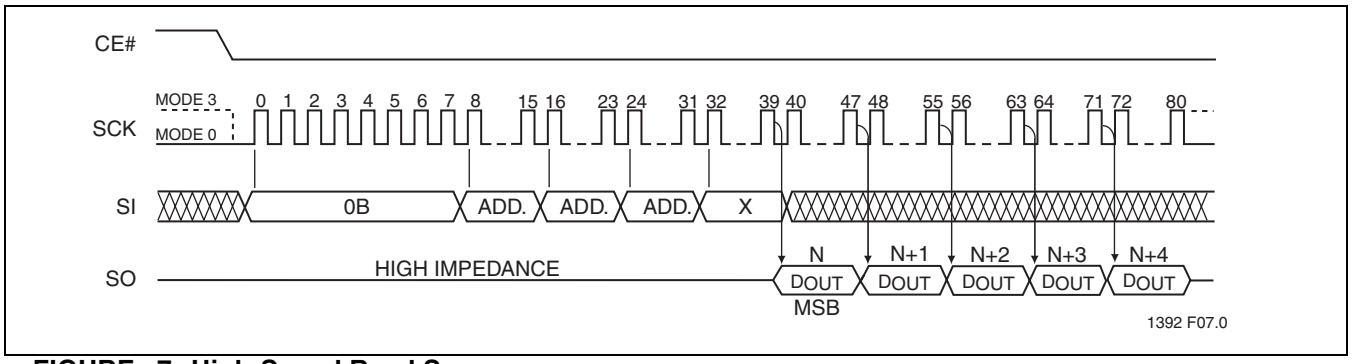

FIGURE 7: High-Speed Read Sequence

Fast-Read Dual-Output (75 MHz)

The Fast-Read Dual-Output (3BH) instruction outputs data up to 75 MHz from the SIO_0 and SIO_1 pins. To initiate the instruction, execute an 8-bit command (3BH) followed by address bits A23-A0 and a dummy byte on SI/SIO_0. Following a dummy cycle, the Fast-Read Dual-Output instruction outputs the data starting from the specified address location on the SIO_1 and SIO_0 lines. SIO_1 outputs, per clock sequence, odd data bits D7, D5, D3, and D1; and SIO_0 outputs even data bits D6, D4, D2, and D0. CE# must remain active low for the duration of the Fast-Read Dual-Output instruction cycle. See Figure 8 for the Fast-Read Dual-Output sequence.

The data output stream is continuous through all addresses until terminated by a low-to-high transition on CE#. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer automatically increments to the beginning (wrap-around) of the address space. for 64 Mbit density, once the data from address location 7FFFFFH has been read the next output will be from address location 000000H.

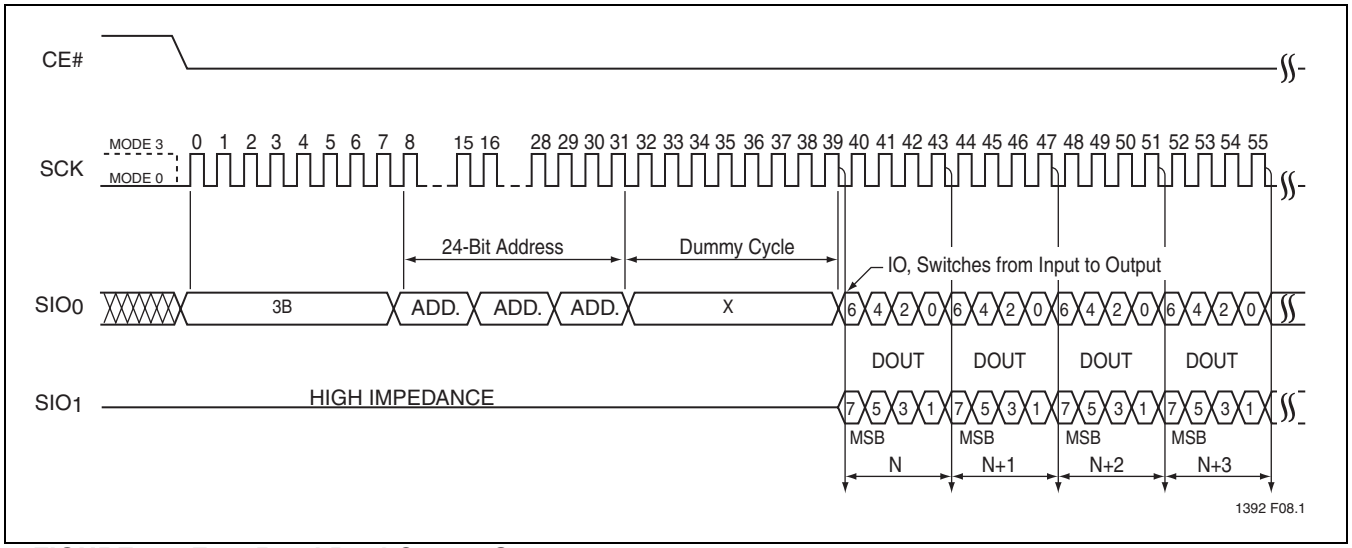

FIGURE 8: Fast-Read Dual Output Sequence